|  |  |  |  |
| --- | --- | --- | --- |
| **Course Code:** | **ECE1002** | **Course Name:** | **Semiconductor Devices and Circuits Lab** |
| **Faculty In – Charge:** | **Dr. Pradeep Naryanan. S.** | **Department:** | **SENSE** |
| **Name of the Student:** | **Aryan Pandey** | **Registration Number:** | **20BLC1087** |
| **Experiment No.:** | **8** | **Date of Experiment:** | **17.05.2021** |
| **Name of the Experiment:** | **DESIGN AND VERIFIY THE CIRCUIT TO MEASURE AND PLOT THE DC AND AC LOAD-LINE ANALYSIS OF A TRANSISTOR** | | |

**OBJECTIVE:**

To design and verify the behaviour of DC and AC load-line analysis of a transistor using LTSPICE Simulator and observe its characteristics.

**TOOLS:**

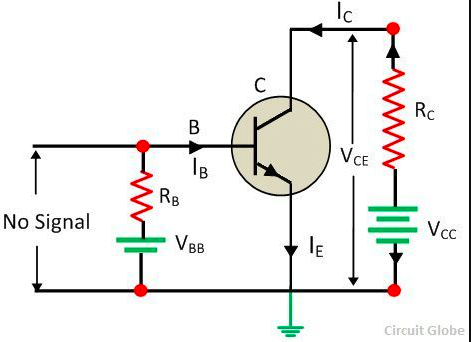
LTSPICE XVII Simulator.

**THEORY**

DC LOAD LINE ANALYSIS

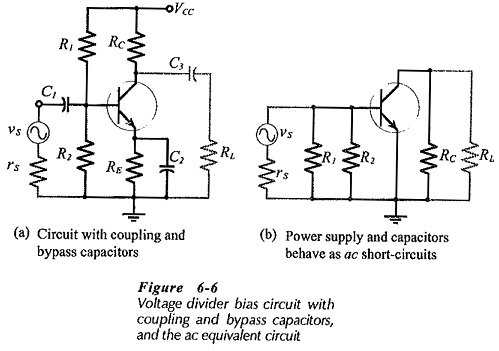
The DC load represents the desirable combinations of the collector current and the collector-emitter voltage. It is drawn when no signal is given to the input, and the transistor becomes bias.

Consider a CE NPN transistor circuit shown in the figure below where no signal is applied to the input side. For this circuit, DC condition will obtain, and the output characteristic of such a circuit is shown in the figure below.



AC LOAD LINE ANALYSIS:

Capacitors behave as short-circuits to ac signals, so in the ac equivalent circuit for a transistor circuit all capacitors must be replaced with short-circuits. Power supplies also behave as ac short-circuits, because the dc supply voltage is not affected by ac signals. Also, all power supplies have large-value capacitors at the output terminals, and these will offer short-circuits to ac signals. Substituting short-circuits in place of the power supply and all capacitors in the circuit in Fig. 6-6(a) gives the ac equivalent circuit in Fig. 6-6(b). If RL is present, as shown, it appears in parallel with RC in the ac equivalent circuit of AC Load Line of BJT.



**PROCEDURE**

CONSTRUCTION FOR BOTH DC LOAD AND AC LOAD ARE BOTH SAME:

CONSTRUCTION PROCEDURE:

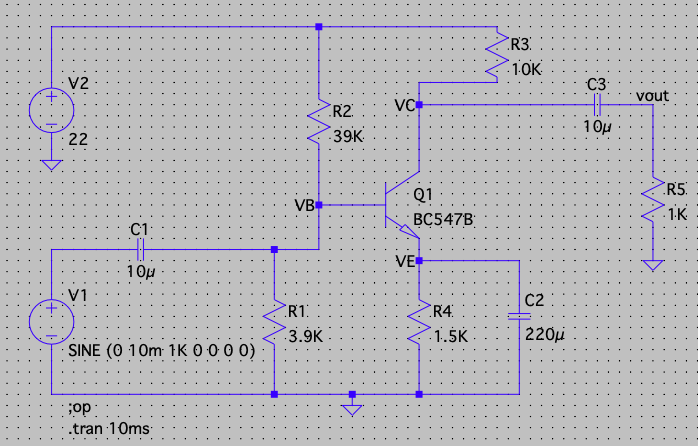
* We are using transistor “BC 547B”. draw a NPN Transistor pick a new transistor and choose a suitable transistor
* Take two voltmeters , fix one voltmeter to 22V and the other voltmeter let us do AC and DC load analysis respectively later on.
* Take three resistors of 39 kΩ, 1.5 kΩ, 3.9 kΩ and 1 kΩ
* Take 3 capacitors of 10 µF, 220 µF and 10 µF
* Take two grounds.
* Name label VOUT and VIN
* Arrange the 2 grounds after choosing .

For DC Analysis: -

Sine Simulation: -

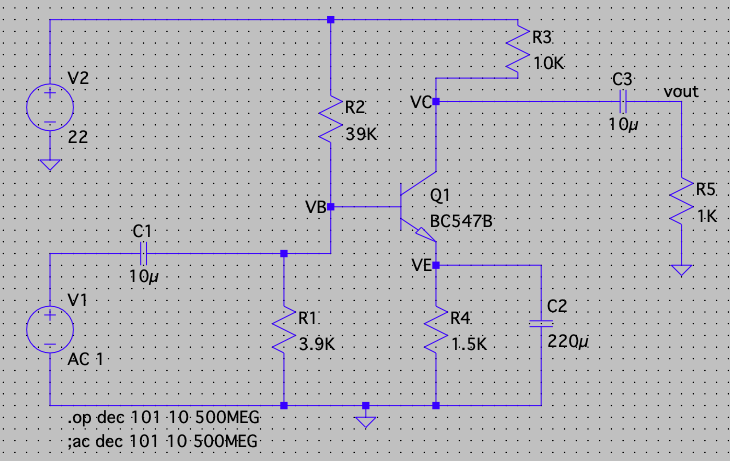
* The Voltmeter which provides the input, needs to be set.
* Click on edit Simulation Command
* Set the ac analysis in sine as shown above, also select “;op” for the analyisis

Arrange your circuit in the following way: -



AC Load Line Analysis: -

1. The voltmeter which provides the input, needs to be set.
2. Click on edit simulation command
3. Now perform dc sweep analysis in LT Spice to plot input characteristics.
4. Now, click on the simulate button and select simulation command. then from the pop-up window select “dc sweep”.
5. Here you need to select the option ” first source” since we are plotting the input characteristics.
6. So, enter the values for the below parameters. refer the below screen.
7. Under first source: -
   * Name of first voltage source - 101
   * Type of Sweep - Decade
   * Start Value - 10
   * Stop Value - 500MEG
8. Right Click on the voltmeter-click on the none check box.
9. Set AC amplitude to 1.



Arrange the circuit as shown above:

Input - Output for both AC and DC analysis of load in transistors please your curser on the vin label for the input and place your cursor on the VOUT label for VOUT.

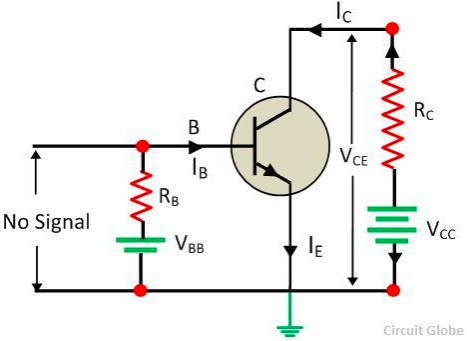
(A) Verification of DC Load Line Analysis

(NPN Transistor): -

DC Load Analysis: -

The DC load represents the desirable combinations of the collector current and the collector-emitter voltage. It is drawn when no signal is given to the input, and the transistor becomes bias.

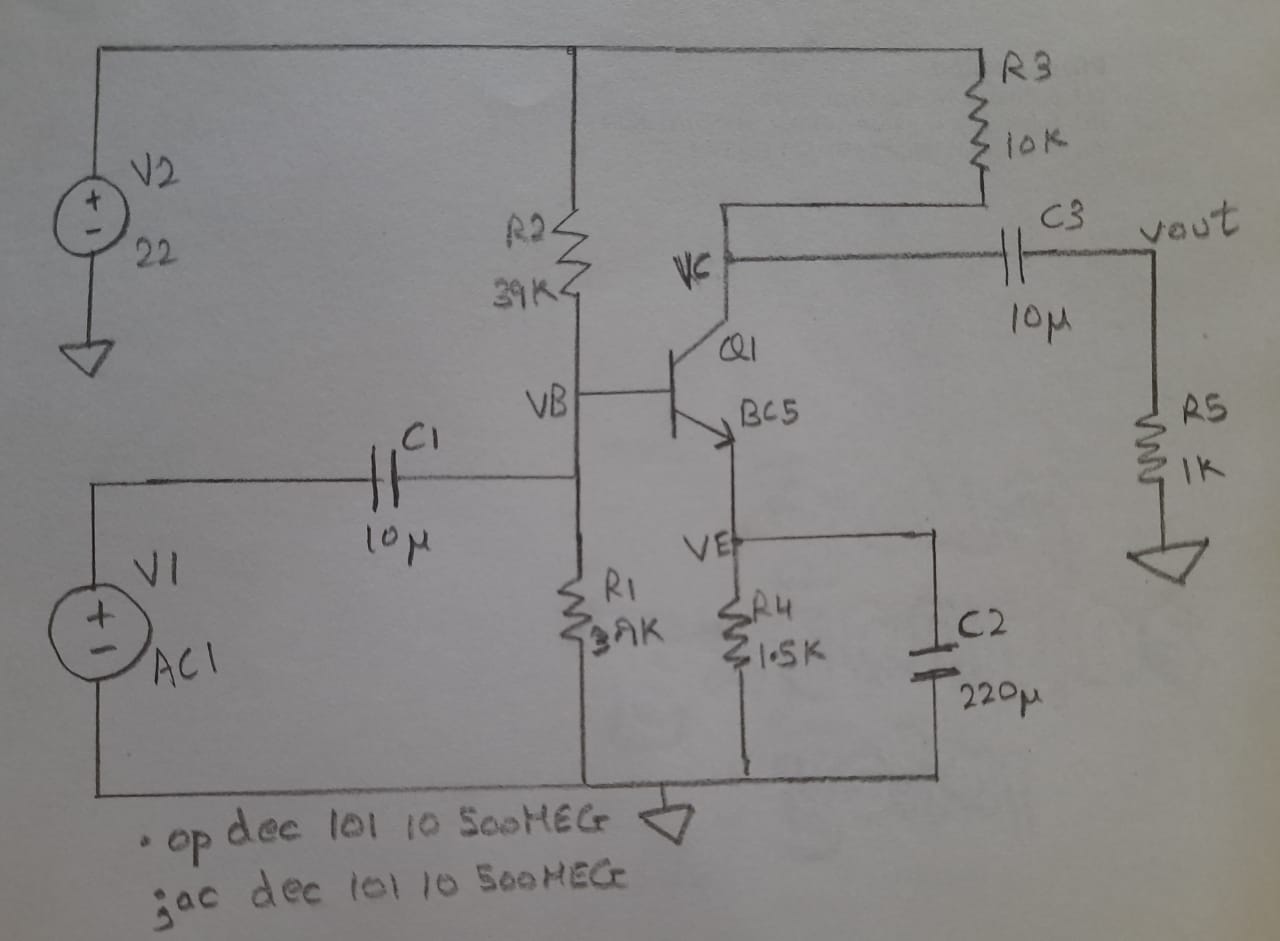
Consider a CE NPN transistor circuit shown in the figure below where no signal is applied to the input side. For this circuit, DC condition will obtain, and the output characteristic of such a circuit is shown in the figure below.



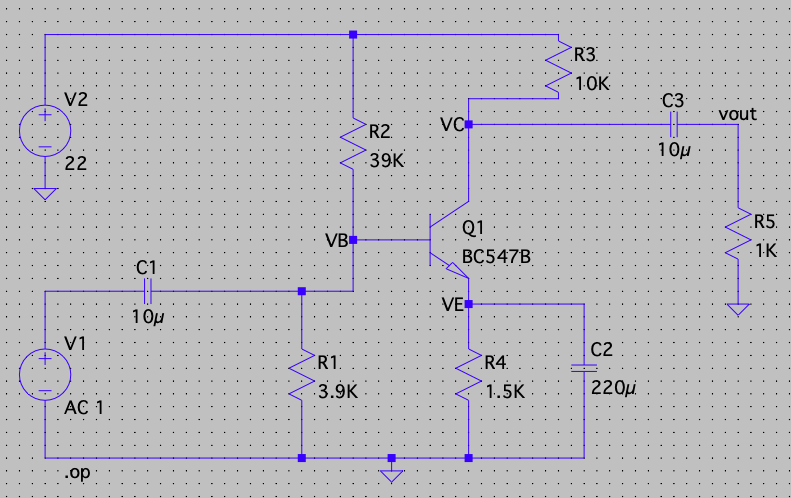
Components Required: -

* Voltmeter
* Resistors
* Capacitors
* Ground
* Wires

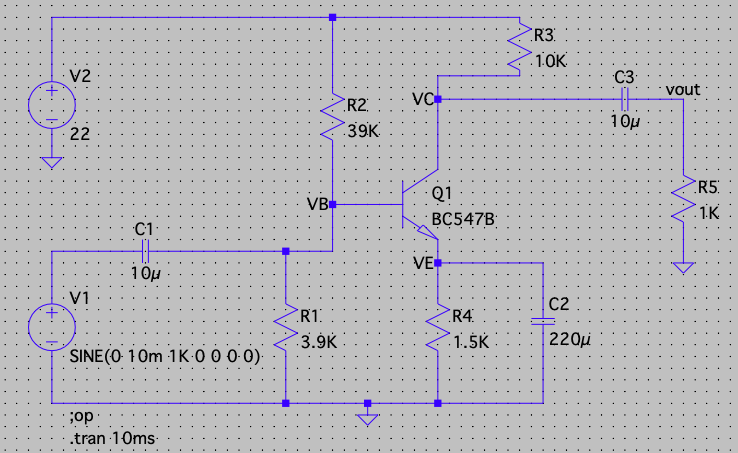
Logic Diagram: -



Simulator Diagram – Schematic:

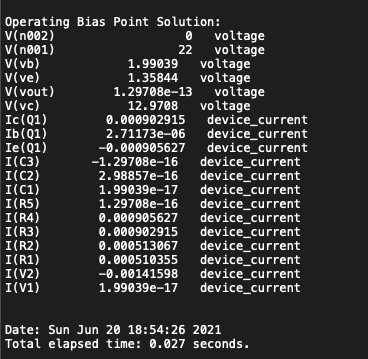


AND



Waveform: -

Output: -

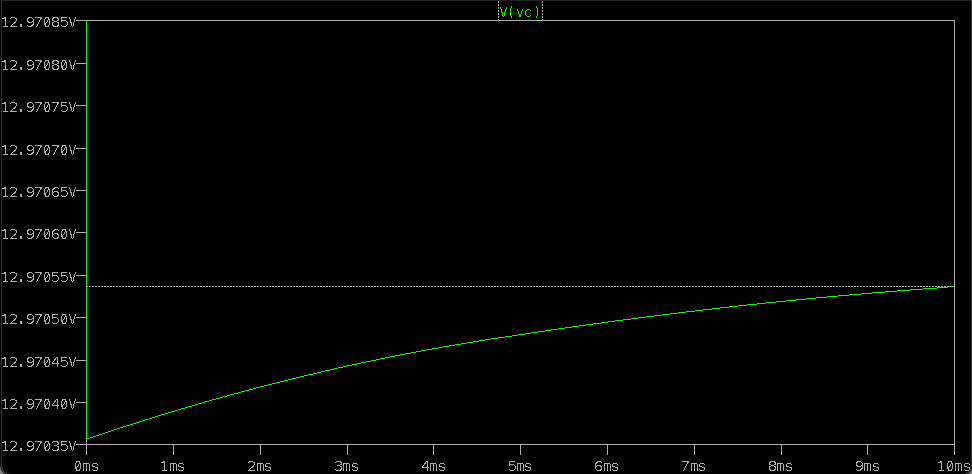


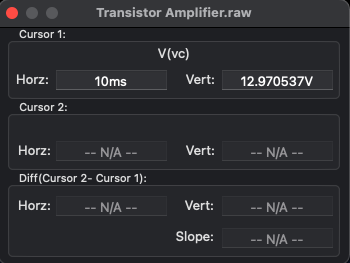
VB = 1.99039

VC = 12.9708

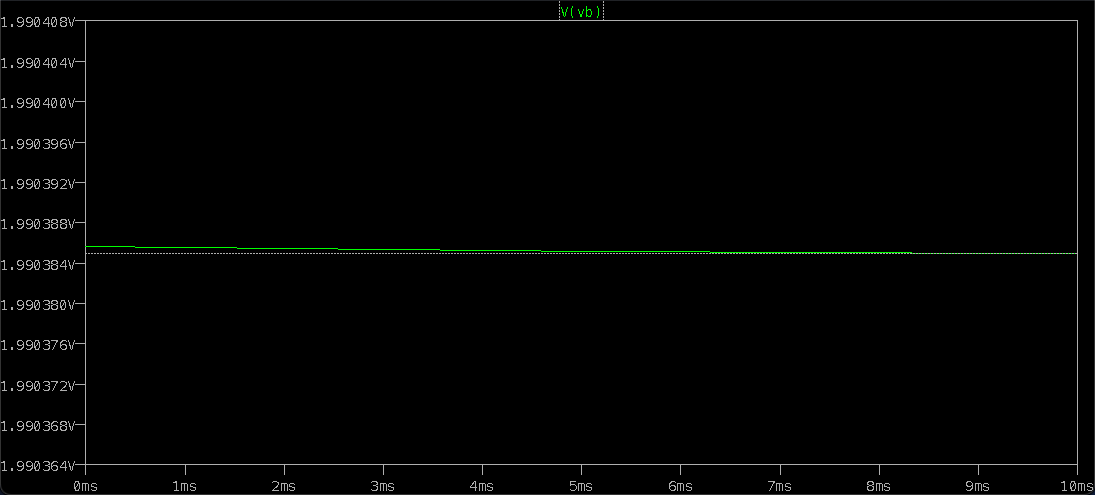
VE = 1.35844

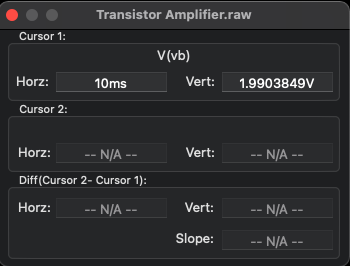
VC = OUTPUT WAVEFORM: -

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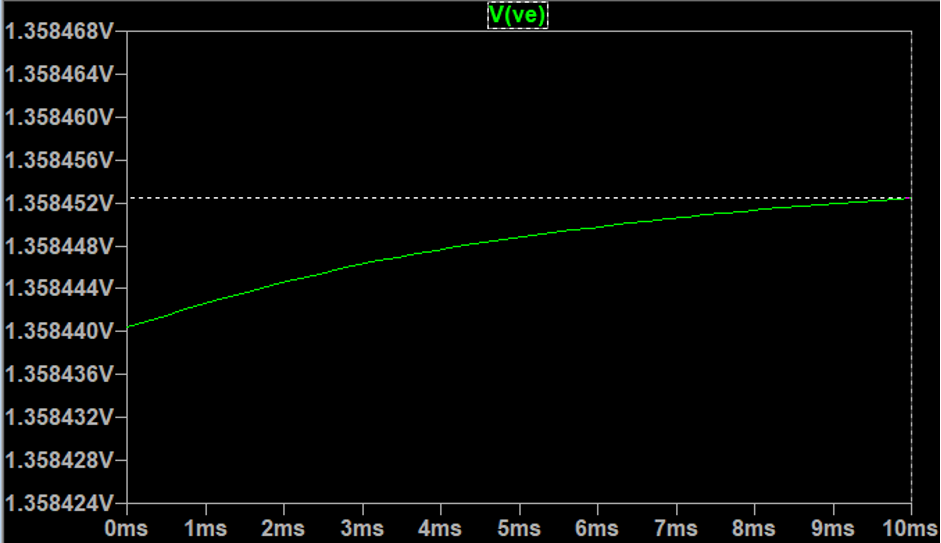


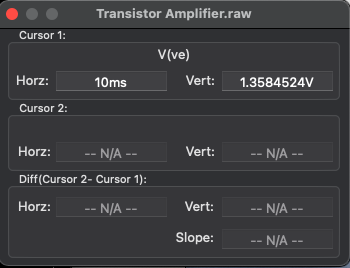
VB = Output Waveform: -



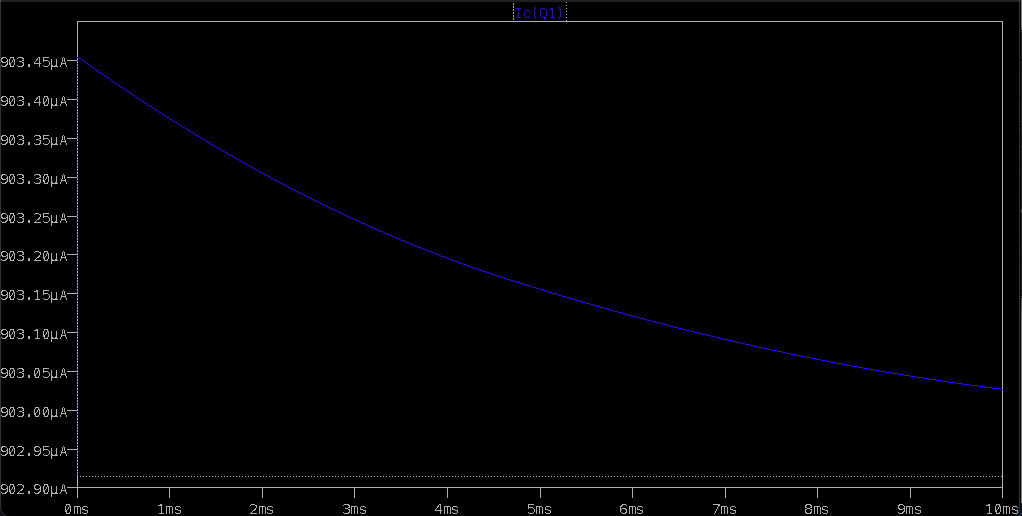


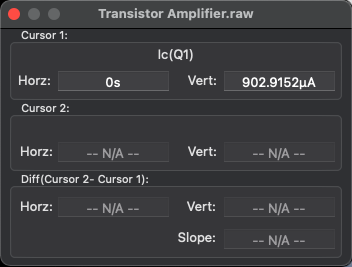
VE = Output Waveform: -

****

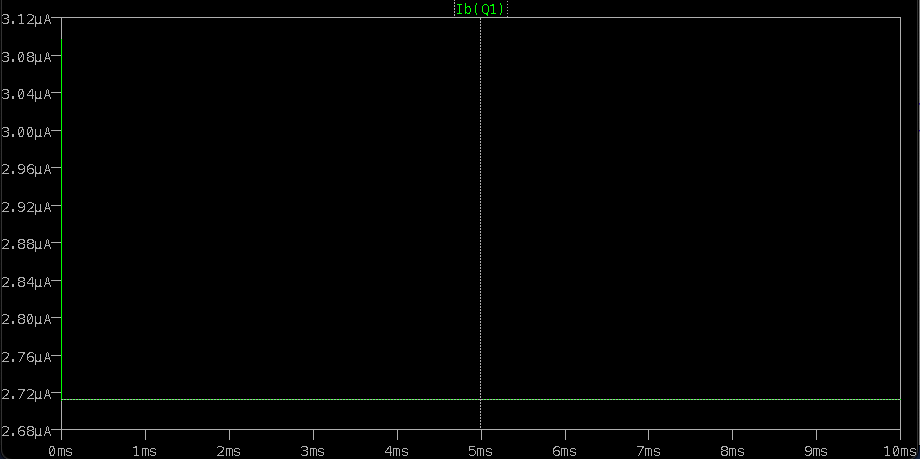


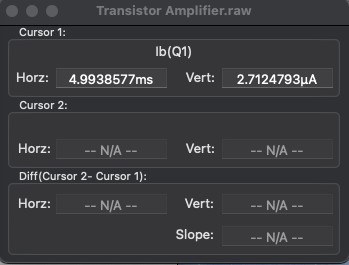
IC Value: -



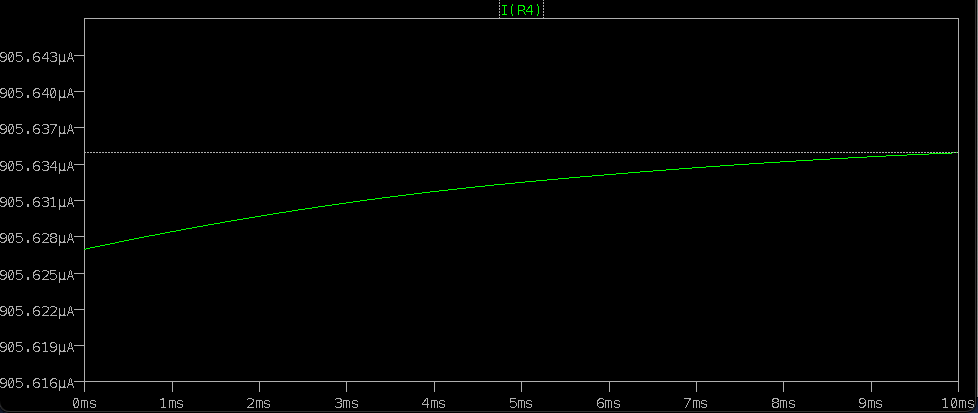


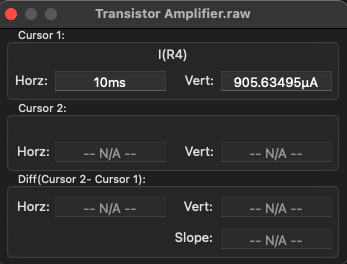
IB Value: -





IE/I R4 Value: -



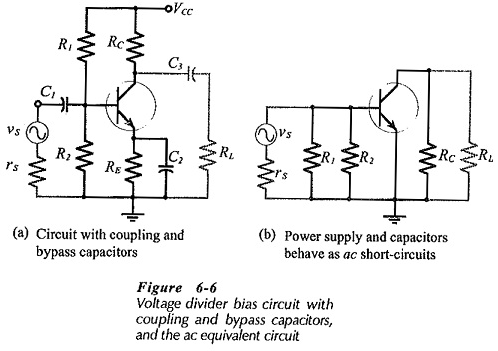
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(B) Verification of AC Load Line Analysis

(NPN transistor): -

AC LOAD LINE ANALYSIS:

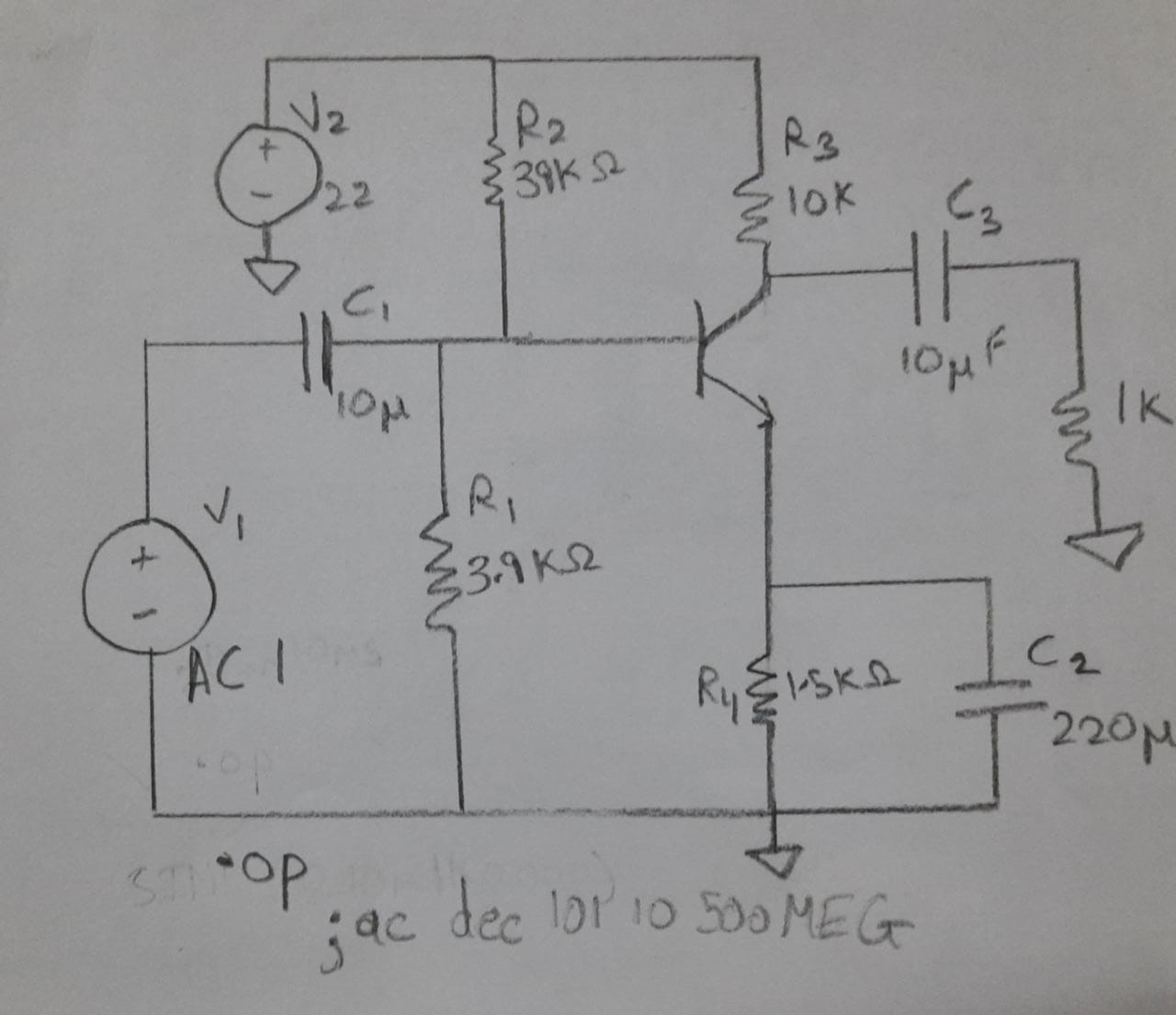
Capacitors behave as short-circuits to ac signals, so in the ac equivalent circuit for a transistor circuit all capacitors must be replaced with short-circuits. Power supplies also behave as ac short-circuits, because the dc supply voltage is not affected by ac signals. Also, all power supplies have large-value capacitors at the output terminals, and these will offer short-circuits to ac signals. Substituting short-circuits in place of the power supply and all capacitors in the circuit in Fig. 6-6(a) gives the ac equivalent circuit in Fig. 6-6(b). If RL is present, as shown, it appears in parallel with RC in the ac equivalent circuit of AC Load Line of BJT.



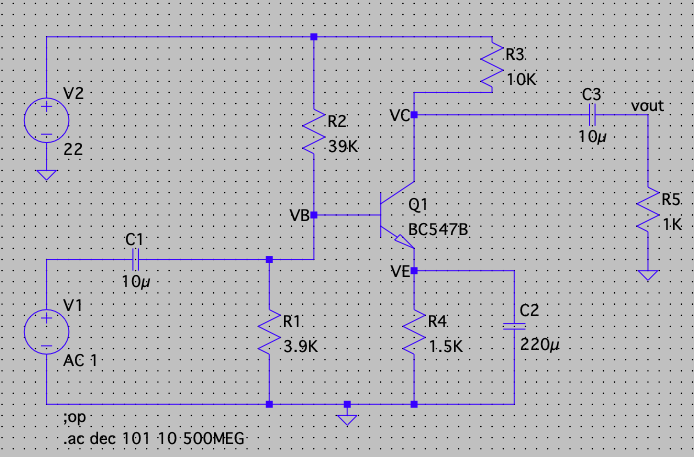
Components Required: -

* Voltmeter
* Resistors
* Capacitors
* Ground
* Wires

Logic Diagram: -

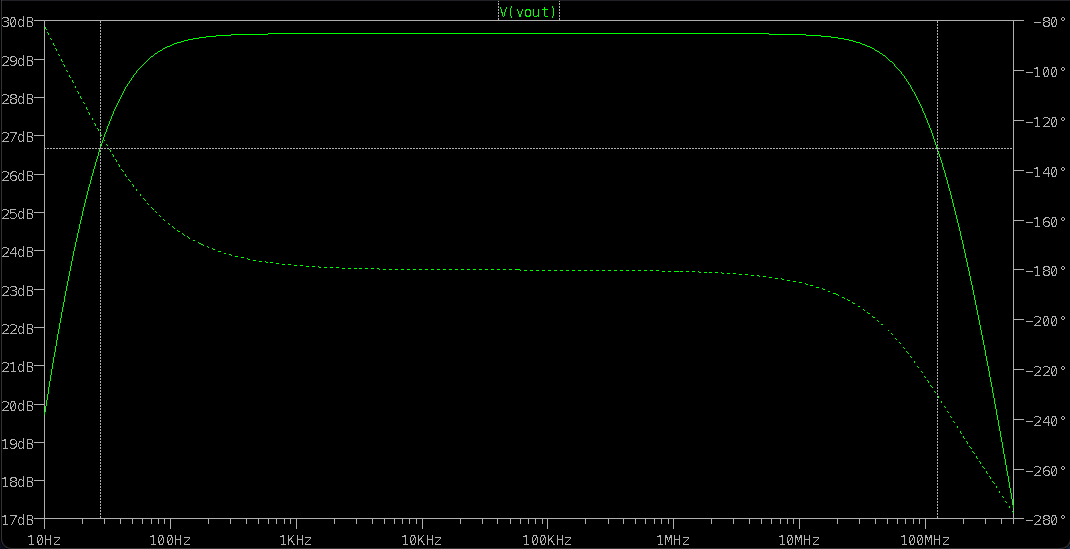


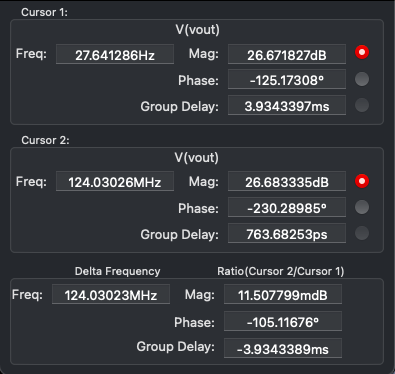
Simulator Diagram – Schematic:



Waveform: -

Output: -



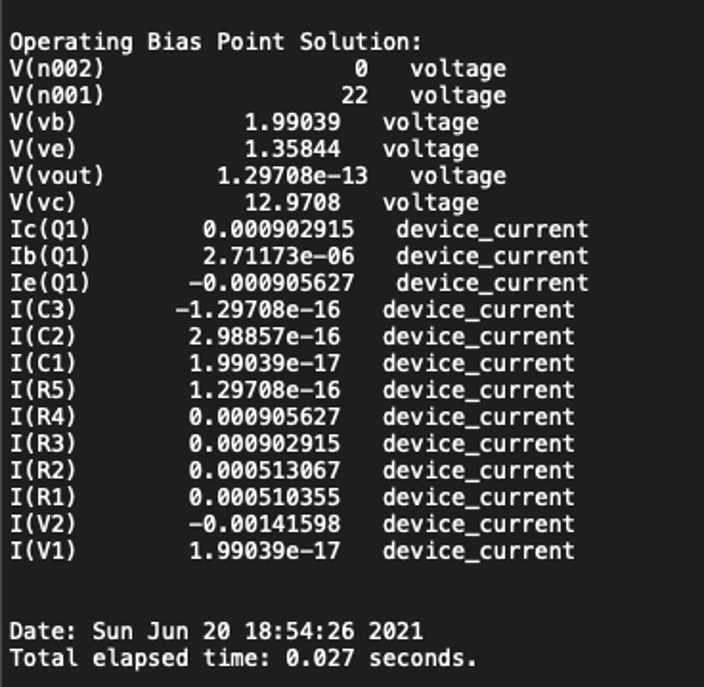


Gain in Decibels = 29.669 dB

Phase Shift = -180 Degree

Calculations:

DC Analysis: -

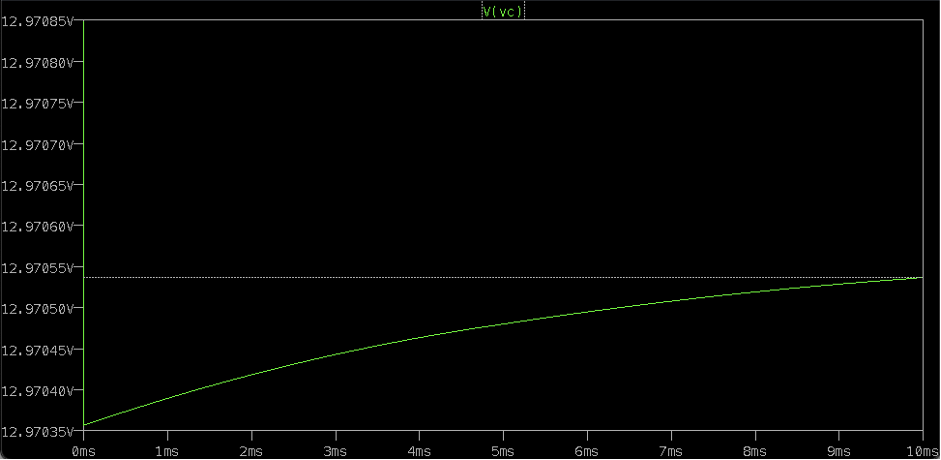


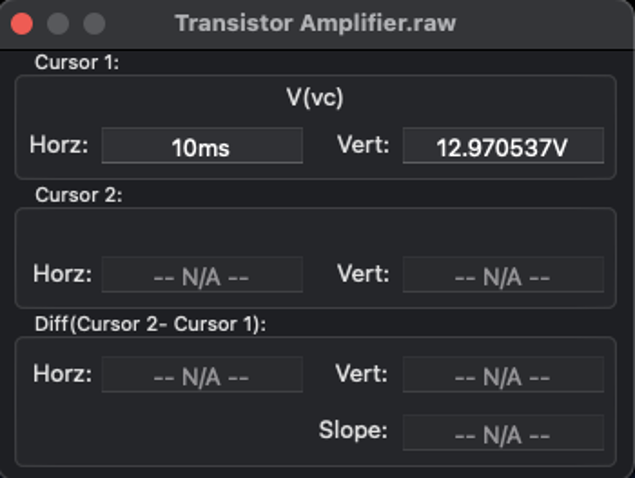
VB = 1.99039

VC = 12.9708

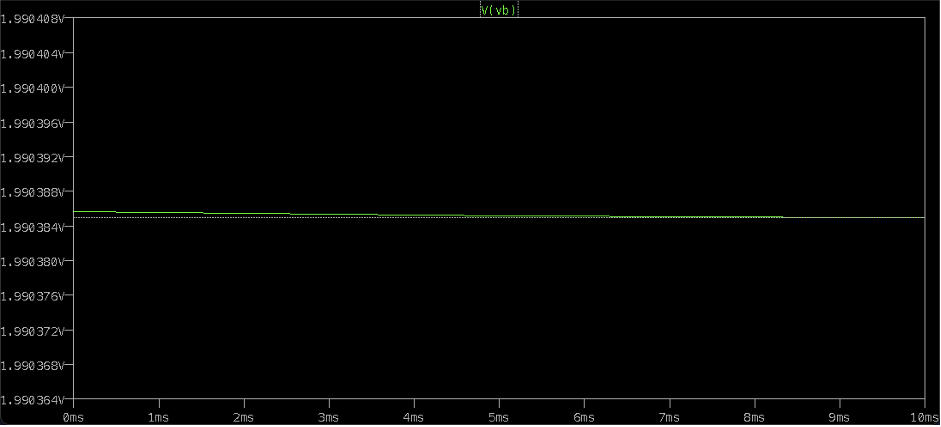
VE = 1.35844

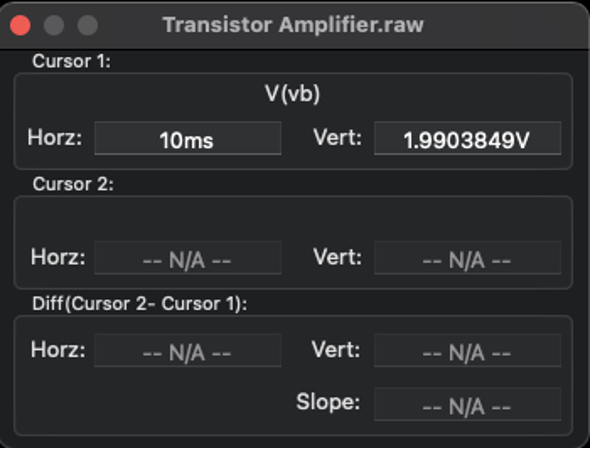
VC = Output Waveform: -



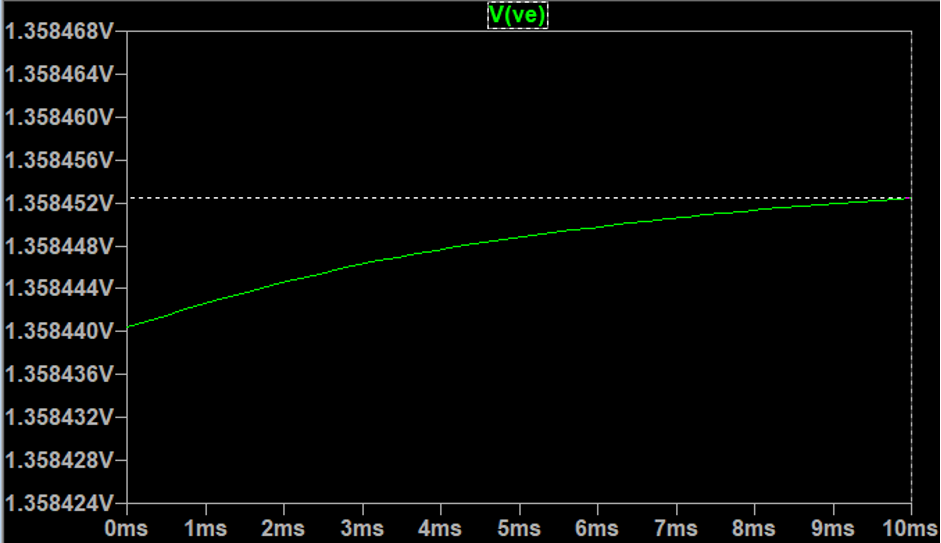


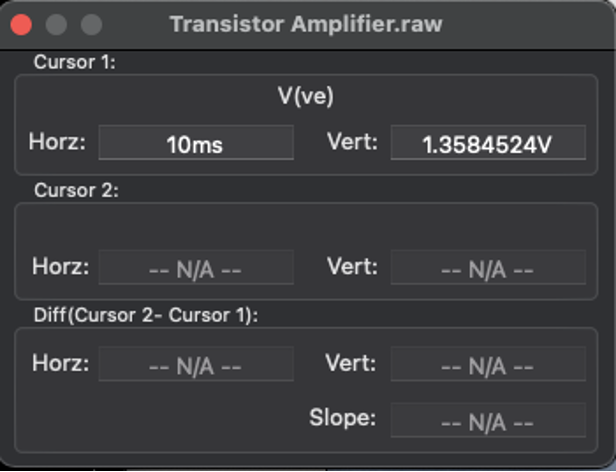
VB = Output Waveform: -



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VE = Output Waveform:





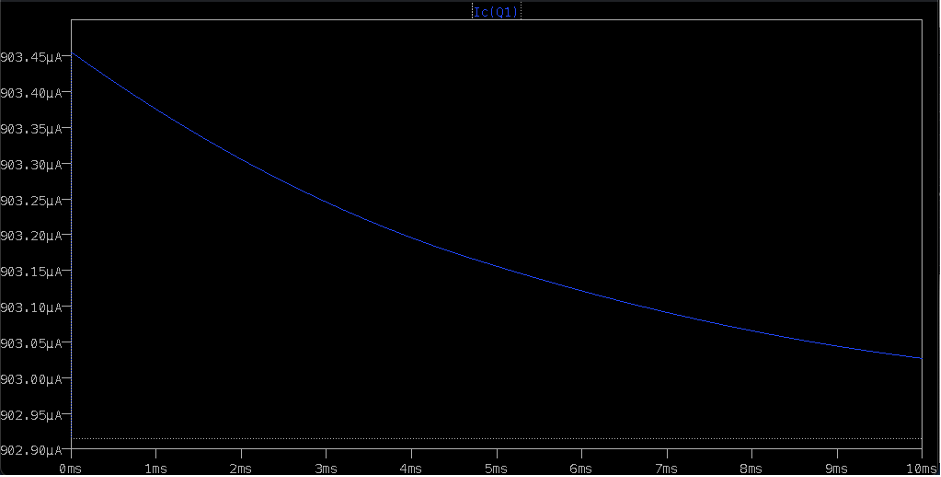
Therefore: -

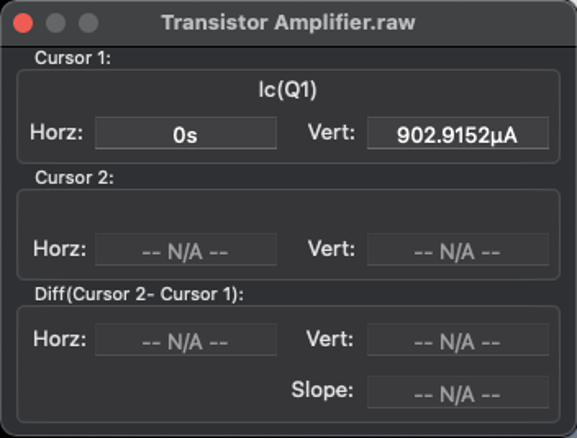
VB = 1.99039

VC = 12.9708

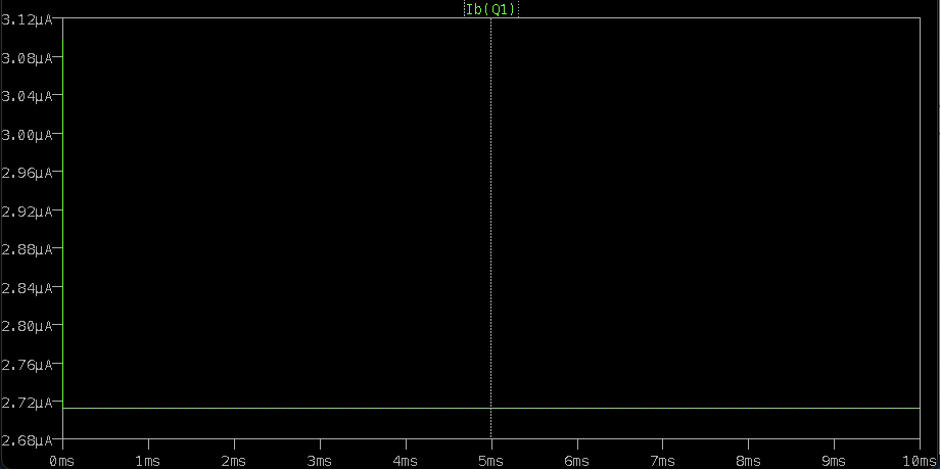
VE = 1.35844

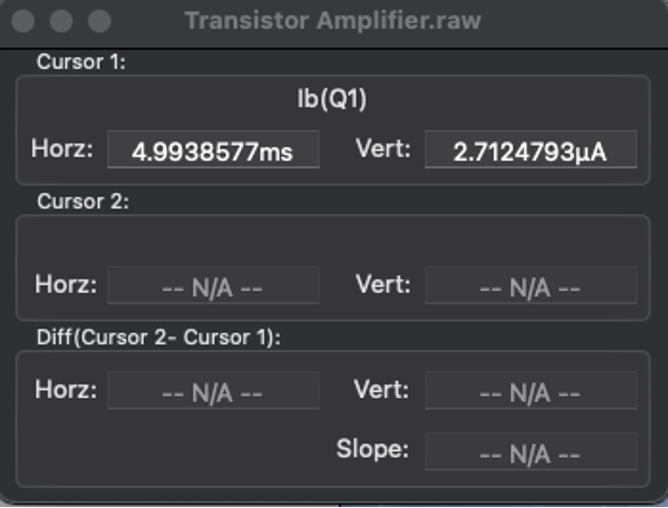
IC Value: 0.000902915 A



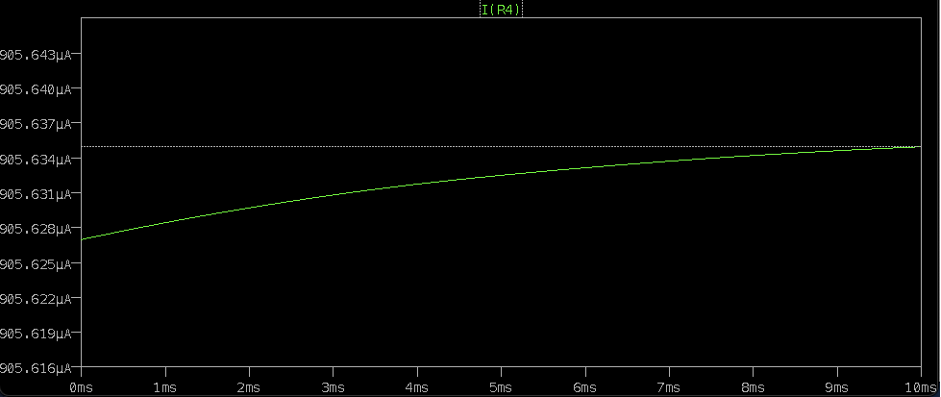


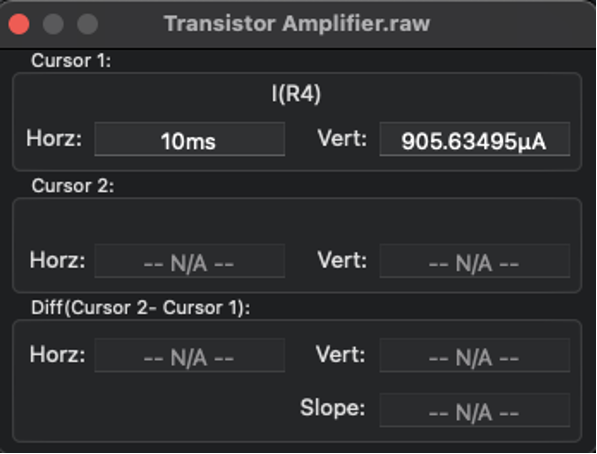
IB Value: 2.7124795 A





IE Value: 905.63495 µA





Calculations for DC:

IC = VCC-VCE/RC

=22-12.9708/1K

=9.0292 mA

=0.00090292 A

Hence verified the current IC.

IE = (VE – 0)/RE

IE = 1.35844/1.5k

= 905.63495µA

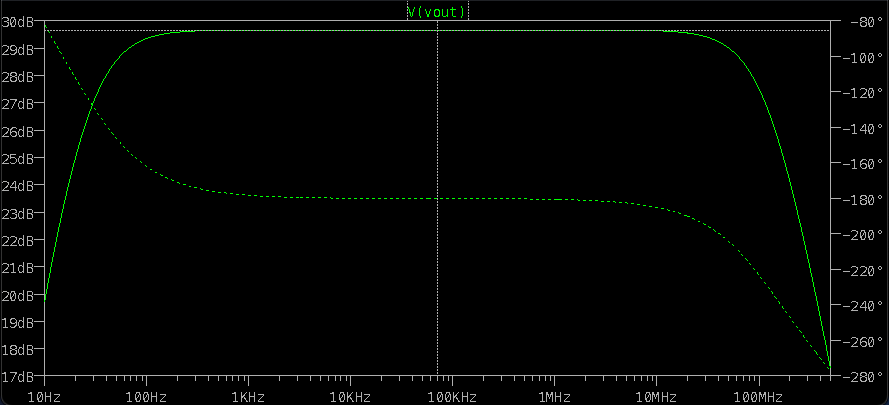
Hence the current IE is verified.

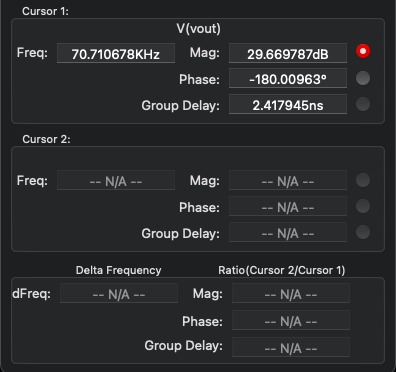
IB = IE = IC

IB = 2.71495 µA

Hence verified the current IB.

IN AC ANALYIS: -

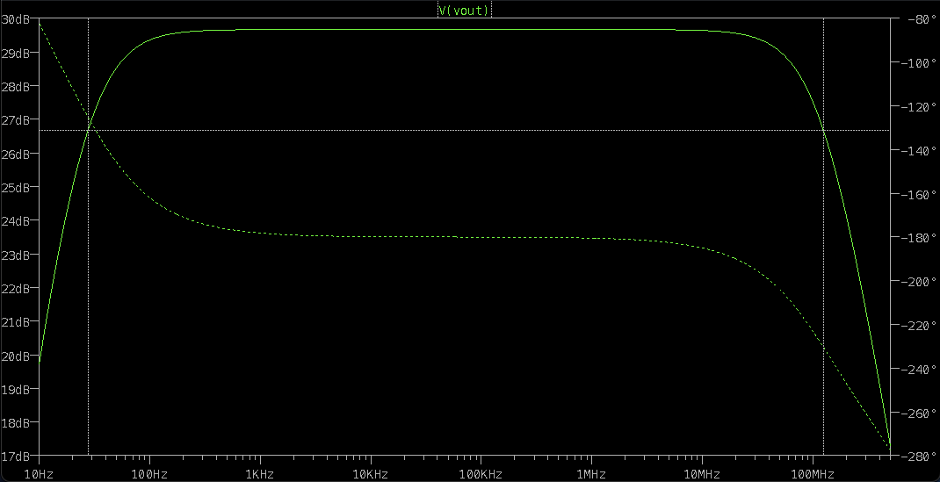


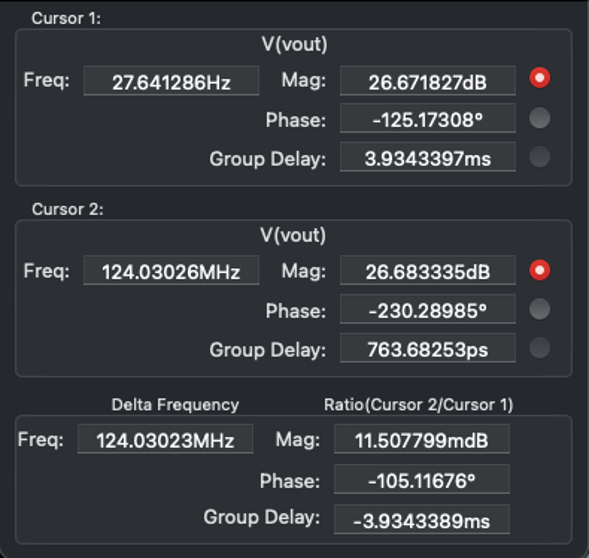


Gain in Decibels = 29.669 dB

Phase Shift = -180 degree

3dB less than 29.669 = 26.669





Therefore Bandwidth = |f1-f2|

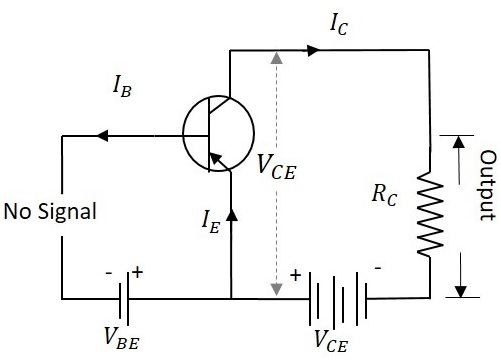
= 124.24939 mhz - 27.724333 hz

= 96.525057 hz

**INFERENCE**

DC Load Line

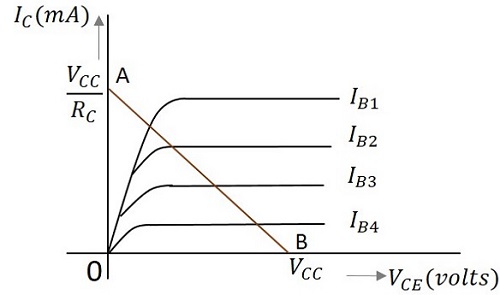
When the transistor is given the bias and no signal is applied at its input, the load line drawn under such conditions, can be understood as **DC** condition. Here there will be no amplification as the **signal is absent**. The circuit will be as shown below.



The value of collector emitter voltage at any given time will be

VCE = VCC − ICRC

As VCC and RC are fixed values, the above one is a first degree equation and hence will be a straight line on the output characteristics. This line is called as **D.C. Load line**. The figure below shows the DC load line.



To obtain the load line, the two end points of the straight line are to be determined. Let those two points be A and B.

To obtain A: -

When collector emitter voltage VCE = 0, the collector current is maximum and is equal to VCC/RC. This gives the maximum value of VCE. This is shown as

VCE = VCC − ICRC

0 = VCC − ICRC

IC = VCC/RC

This gives the point A (OA = VCC/RC) on collector current axis, shown in the above figure.

To obtain B: -

When the collector current IC = 0, then collector emitter voltage is maximum and will be equal to the VCC. This gives the maximum value of IC. This is shown as

VCE = VCC − ICRC

VCE = VCC (As IC = 0)

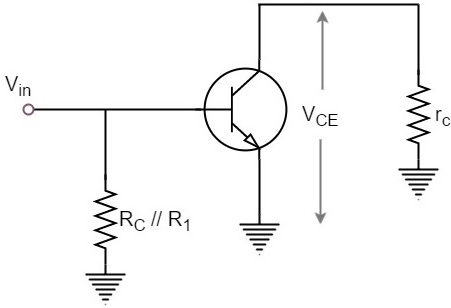
This gives the point B, which means (OB = VCC) on the collector emitter voltage axis shown in the above figure.

Hence we got both the saturation and cut - off point determined and learnt that the load line is a straight line. So, a DC load line can be drawn.

AC Load Line: -

The DC load line discussed previously, analyses the variation of collector currents and voltages, when no AC voltage is applied. Whereas the AC load line gives the peak-to-peak voltage, or the maximum possible output swing for a given amplifier.

We shall consider an AC equivalent circuit of a CE amplifier for our understanding.



From the above figure,

VCE = (RC/R1) X ICVCE = (RC/R1)×IC

RC = RC/R1

For a transistor to operate as an amplifier, it should stay in active region. The quiescent point is so chosen in such a way that the maximum input signal excursion is symmetrical on both negative and positive half cycles.

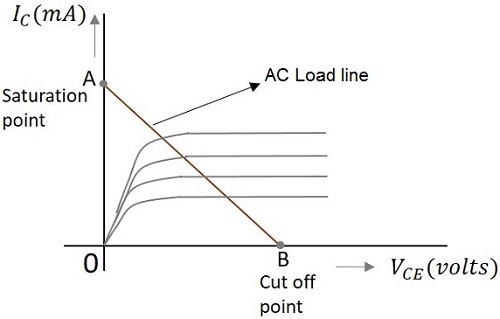
Hence,

VMAX = VCEQ

VMIN = −VCEQ

Where VCEQ is the emitter - collector voltage at quiescent point

The following graph represents the AC load line which is drawn between saturation and cut off points.



From the graph above, the current IC at the saturation point is

IC (sat) = ICQ + (VCEQ/RC)

The voltage VCE at the cut - off point is

VCE(off) = VCEQ + ICQRC

Hence the maximum current for that corresponding VCEQ is

ICQ = ICQ ∗ (RC/R1)ICQ=ICQ ∗ (RC/R1)

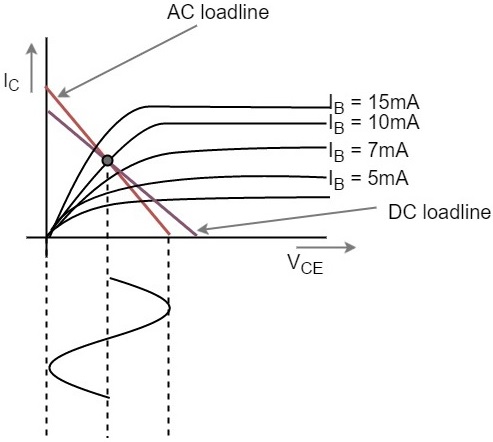
Hence by adding quiescent currents the end points of AC load line are

IC(SAT) = ICQ + VCEQ/(RC/R1)

VCE(off) = VCEQ + ICQ ∗ (RC/R1)

AC and DC Load Line: -

When AC and DC Load lines are represented in a graph, it can be understood that they are not identical. Both of these lines intersect at the Q-point or quiescent point. The endpoints of AC load line are saturation and cut off points. This is understood from the figure below.



From the above figure, it is understood that the quiescent point (the dark dot) is obtained when the value of base current IB is 10mA. This is the point where both the AC and DC load lines intersect.

**RESULT:**

**SUCCESSFULLY DESIGNED AND VERIFIED THE CIRCUIT TO MEASURE AND PLOT THE DC AND AC LOAD-LINE ANALYSIS OF A TRANSISTOR**